Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A flash memory comprising:

a sector of memory cells formed on a first ion well of first conductivity type in a substrate of the first conductivity type;

a second ion well of second conductivity type disposed underneath the first ion well in the substrate; and

an selection transistor located at one end of the sector of memory cells, wherein the selection transistor has a first end electrically connected to a source of each of the memory cells through a sub-bit line and a second end electrically connected to a main bit line, and wherein the source of each of the memory cells consists of a first ion doped region of the first conductivity type and a second ion doped region of the second conductivity type that surrounds the first ion doped region and is short-circuited with the first ion doped region.

[c2] 2. The flash memory of claim 1 wherein the selection transistor is formed within the first ion well.

[c3] 3.The flash memory of claim 2 wherein the selection transistor is a PMOS transistor.

[c4] 4.The flash memory of claim 1 wherein the selection transistor is formed within a third ion well of second conductivity type, and wherein the third ion well substantially abuts upon the first ion well and is formed above the second ion well.

[c5] 5.The flash memory of claim 4 wherein the third ion well is a P-well and the selection transistor is a NMOS transistor.

[c6] 6.The flash memory of claim1 wherein the first conductivity type is N type and the second conductivity type is P type.

[c7] 7.The flash memory of claim 1 wherein the short circuit connection between the first ion doped region and the second ion doped region of the source of each of the memory cells is created by using a metal that penetrates the first ion doped region to the second ion doped region.

[c8] 8.The flash memory of claim 1 wherein the short circuit connection between the first ion doped region and the second ion doped region of the source of each of the memory cells is created by using a metal that connects exposed area of the first ion doped region with exposed area of the second ion doped region.

[c9] 9. The flash memory of claim 1 further comprising a isolation structure disposed on the substrate between the selection transistor and the sector of memory cells.